

| Form 1449A/PTO (Modified)<br>(many sheets as necessary) |                      | Attorney Docket No.:<br>42390.P9429  | Application Number:<br>09/608,637 |
|---|----------------------|--|-----------------------------------|
| Sheet 1 of 1  |                      | First Named Inventor:<br>Jin Yang  | Examiner:<br>Unassigned           |
|   |                      | Filing Date:<br>June 30, 2000  | Art Unit:<br>2763                 |
| <b>OTHER ART - NO PATENT LITERATURE DOCUMENTS</b>       |                      |  |                                   |
| Examiner Initials*                                      | Cite No <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published | Translation <sup>2</sup>          |
| /DC/  |                      | BRADLEY, J., et al., "Compositional BDD Construction: A Lazy Algorithm," Department of Computer Science, University of Bristol, UK, April 6, 1998  |                                   |
| /DC/  |                      | BURCH, E. M., et al., "Symbolic Model Checking for Sequential Circuit Verification," <u>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</u> , Volume 13, Issue 4, April 1994, pp. 401-424  |                                   |
| /DC/  |                      | CAMPOS, S.V.A., "Symbolic Model Checking in Practice," <u>XII Symposium on Integrated Circuits and Systems Design, 1999 Natal, Brazil - IEEE</u> , September 1999, pp. 98-101  |                                   |
| /DC/  |                      | HOJATI, R., et al., "Early Quantification and Partitioned Transition Relations," <u>1999 IEEE International Conference on Computer Design: VLSI in Computers and Processors, 1996. ICCD '96 Proceedings - Austin, TX, October, 1996</u> , pp. 12-19            |                                   |
| /DC/  |                      | ZHANG, ZHANG, "An Approach to Hierarchy Model Checking via Evaluating CTL Hierarchically," <u>Proceedings of the Fourth Asian Test Symposium, 1995 - Bangalore, India, November 1995</u> , pp. 45-49   |                                   |
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| Examiner Signature | /Dwin Craig/ (10/15/2007) | Date Considered |  |
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